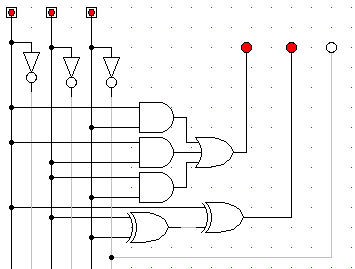
1) Design a combinational circuit with three inputs x, y, z, and three outputs a, b, and

c. When the binary input is 0, 1,2, or 3 , the binary output is 1 greater than the

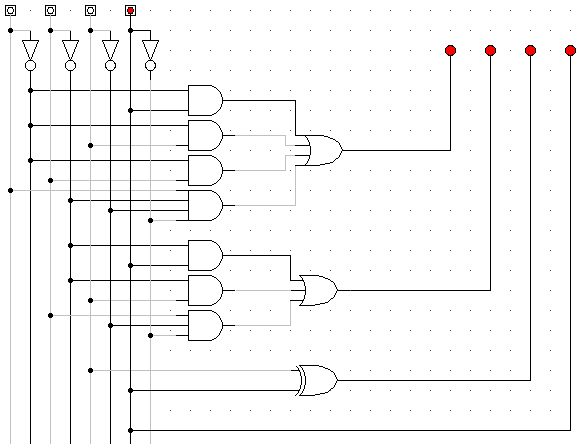
input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the

input. (10 Marks)



2) Design a 4bits combinational circuit 2’s complementer (the output generates the

2’s complement of the input binary number).(10 Marks)



3) show that the characteristic equation for the complement output of a JK flip flop

is (10 Marks)

**Q’(t+1) = J’Q’ + KQ**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q(t) | J | K | Q(t+1) | Q’(t+1) |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| JK | 00 | 01 | 11 | 10 |
| Q | // | // | // | // |
| 0 | 1 | 1 |  |  |
| 1 |  | 1 | 1 |  |

=(J’Q’)+(JK)

4) A sequential circuit with two D flip flops A and B, two inputs x and y and one

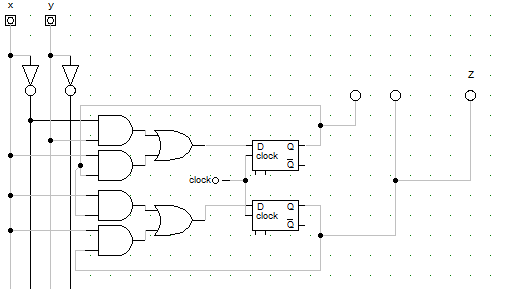
output z is specified by the following next state and output equation (10 Marks)

**A(t+1) = x’y + xA**

**B(t+1) = x’B + xA**

**z = B**

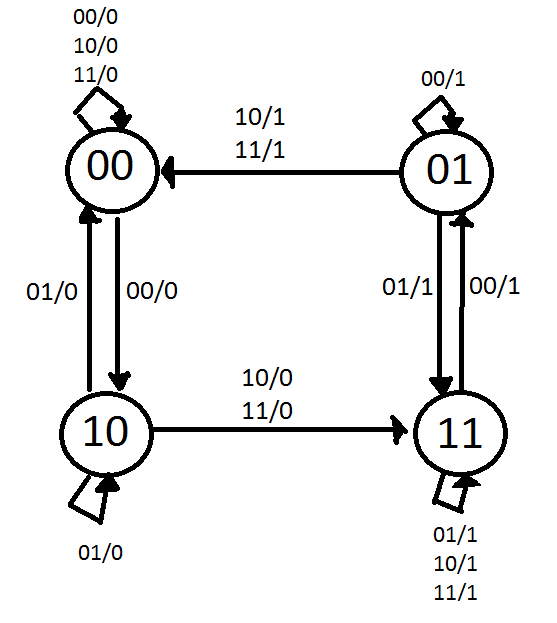
1. Draw the logic diagram of the circuit



1. List the state table for the sequential circuit

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| X | Y | A(t) | B(t) | A(t+1) | B(t+1) | Z |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

1. Draw the corresponding state diagram

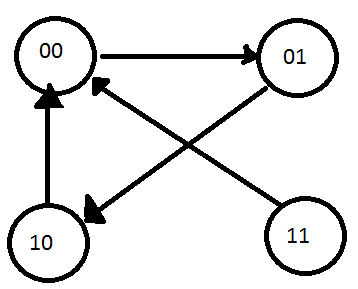


5) Drive the state table and the state diagram of the sequential circuit shown below:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A(t) | B(t) | Ta | Tb | A(t+1) | B(t+1) |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |

Ta=(A+B)

Tb=(A’+B)



6) A sequential circuit has two JK flip flops A, and B and one input X. The circuit is

described by the following flip flop equations. (10 Marks)

**JA = x KA = B’**

**JB = x KB = A**

1. Derive the state equations A(t+1) and B(t+1).

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| X | A(t) | B(t ) | Ja | Ka | Jb | Kb | A(t+1) | B(t+1) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB | 00 | 01 | 11 | 10 |
| X | // | // | // | // |
| 0 |  |  | 1 |  |
| 1 | 1 | 1 | 1 |  |

A(t+1)=xA’(t)+A(t)B(t)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB | 00 | 01 | 11 | 10 |
| X | // | // | // | // |
| 0 |  | 1 |  |  |
| 1 | 1 | 1 |  | 1 |

B(t+1)= A(t)B(t)+ xB’(t)

1. Draw the state diagram of the circuit

